IN THE DRAWINGS

Please find enclosed a replacement for Fig. 6, in which one of the labels has been corrected, as indicated in red, so that the label is consistent with the last paragraph of page 10 of the specification.

IN THE CLAIMS

Please amend the claims below as follows:

A1

1. (AMENDED) Apparatus for enabling an instruction to control data flow bypassing hardware within a processor of a programmable processing engine, the apparatus comprising:

a pipeline of the processor, the pipeline having a plurality of stages including instruction decode, writeback and execution stages, the execution stage having a plurality of parallel execution units; and

an instruction set of the processor, the instruction set defining a register decode value, that specifies one of a first register decode value which defines source operand bypassing, and a second register decode value that defines result bypassing from a previous instruction executing in pipeline stages of the processor.

A2 Sub C1

3. (AMENDED) The apparatus of Claim 2 wherein the register decode value comprises:

said second register decode value is a result bypass (RRB) operand and said first register decode value is an inter-unit result bypass (RISB) operand, each of which explicitly controls data flow within the pipeline of the processor.

A3

9. (AMENDED) A method for enabling an instruction to control data flow bypassing hardware within a pipelined processor of a programmable processing engine, the method comprising the steps of:

defining a register decode value that specifies one of a first register decode value which defines source operand bypassing and a second register decode value that defines result bypassing from a previous instruction executing in pipeline stages of the processor; and

identifying a pipeline stage register for use as a source operand in an instruction containing the register decode value.

A3

10. (AMENDED) The method of Claim 9 further comprising the step of explicitly controlling data flow within the pipeline stages of the processor through the use of a register result bypass (RRB) operand in said second register decode value.

A4

13. (AMENDED) The method of Claim 12 wherein the step of identifying further comprises the steps of:

explicitly specifying the pipeline stage register to be used as the source operand for the instruction.

14. (AMENDED) The method of Claim 13 further comprising:

encoding the RRB operand in fewer bits than a regular register operand.

sub C3

15. (AMENDED) The method of Claim 14 further comprising:

sharing source operand data among the parallel execution units of the pipelined processor through the use of a source bypass (RISB) operand in said first register decode value.

A5

19. (AMENDED) A computer readable medium containing executable program instructions for enabling an instruction to control data flow bypassing hardware within a pipelined processor of a programmable processing engine, the executable program instructions comprising program instructions for:

defining a register decode value that specifies one of a first register decode value that defines source operand bypassing and a second register decode value that defines result bypassing from a previous instruction executing in pipeline stages of the processor; and

identifying a pipeline stage register for use as a source operand in a current instruction containing the register decode value.

Please add the following claims:

20. (NEW) A processor comprising:

an execution unit having an input and an output;

an input register connected to said input and said output of said execution unit; and

a register decode value that specifies bypassing data from said output of said execution unit to said input register during a write back cycle transferring said data to a register file.

21. (NEW) The processor of claim 20 further comprising:

a first instruction having at least one first source operand and a first destination operand;

a second instruction having at least one second source operand and a second destination operand, said at least one second source operand is the same as said first destination operand; and

means for replacing said at least one second source operand with said register decode value.

22. (NEW) The processor of claim 21 further comprising:

means for loading said at least one first source operand from said register file.

23. (NEW) The processor of claim 21 further comprising:

means for loading said at least one first source operand from a memory.

24. (NEW) The processor of claim 21, said means for replacing further comprising:

an instruction decode mechanism.

25. (NEW) The processor of claim 21 further comprising:

said register decode value having fewer bits than said second at least one source operand.

26. (NEW) A processor comprising:

Cont C1

a first execution unit having at least one first input and a first output;

at least one second execution unit having at least one second input and a second output;

A1a

a first input register connected to said at least one first input;

a second input register;

a multiplexer having a first input from said first input register, a second input from said second input register, and an output to said at least one second execution unit; and

a register decode value that specifies bypassing data from said first input register to said at least one second execution unit via said multiplexer.

~~27.~~ 28 (NEW) The processor of claim ~~26~~ 27 further comprising:

29

a first instruction having at least one first source operand and a first destination, said first execution unit processing said first instruction;

a second instruction having at least one second source operand and a second destination operand, said at least one second source operand is the same as said at least one first source operand; and

means for replacing said at least one second source operand with said register decode value.

~~28.~~ 29 (NEW) The processor of claim ~~27~~ 28 further comprising:

30

a register file connected to said first and second input registers; and

means for loading said at least one first and said at least one second source operands from said register file.

~~29.~~ 30 (NEW) The processor of claim ~~27~~ 28 further comprising:

31

a memory connected to said first and second input registers; and

means for loading said at least one first and said at least one second source operands from said memory.

~~30.~~ 31 (NEW) The processor of claim ~~27~~ 28, said means for replacing further comprising:

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